Patent claims

1. Component

- with a chip (CH) bearing component structures, said chip (CH) comprising on one surface solderable metallizations (LM) connected with the component structures (BS),
- with a carrier substrate (TS) which comprises on the lower surface connection areas (KO) for electrically-conductive connection with the component structures of the chip and conductor traces that are connected with the connection areas (AF), whereby the connection areas are respectively at least partially uncovered on the floor of recesses (AN) in the carrier substrate (TS),

whereby the chip (CH) is mounted in flip-chip arrangement by means of bump connections (BU) arranged in the recesses (AN), said bump connections (BU) electrically-conductively connecting the solderable metallizations (LM) to the chip and the connection areas (AF) to the carrier substrate (TS), and whereby the chip at least partially rests on the carrier substrate.

2. Component according to claim 1,

with a multi-layer carrier substrate (TS) which comprises at least an upper and a lower layer (OS, US), and whereby the connection areas (AF) are arranged on the surface of the lower layer.

3. Component according to claim 1,

in which solderable contacts that are arranged on the underside of the carrier substrate over the recesses are sealed below in the recesses (AN) in the carrier substrate (TS).

---

4. Component according to any of the claims 1 through 3,

in that the chip (CH) is fashioned on a piezoelectric substrate as a SAW component, as an FBAR resonator, as a BAW resonator or as an SCF filter.

5. Component according to claim 4,
in that, on the chip (CH) or carrier substrate (TS), a frame (RA) is provided such that a part of the component structures (BS) is arranged in a hollow that is enclosed by the frame and both of the surface of chip and carrier substrate facing it, in that the frame forms the support for the chip or the carrier substrate, and in that the contact area between carrier substrate and chip is circumferentially sealed with a closed solder border (LR).

6. Component according to claim 5,
in that the frame (RA) is formed from plastic or a metallization that is provided on the chip (CH) or the carrier substrate (TS), or in that the frame is the boundary of a depression (VT) provided on the carrier substrate (TS), the depth (h2) of which corresponds to at least the height of the component structures (BS) arranged in the hollow.

7. Component according to claim 5 or 6,
in that the frame (RA) is fashioned as a metallization on the surface of the carrier substrate (TS) and is arranged circumferentially along and underneath the chip edge facing the carrier substrate, and
in that the boundary surface between frame and chip (CH) is circumferentially sealed with a closed solder border (LR).

8. Component according to any of the claims 1 through 7,
in that, in the lower layer (US) of the carrier substrate (TS), feedthroughs (DK) are provided that are filled with a conductive material, whereby the surface of the feedthroughs form [sic] the connection areas (AF).

---

9. Component according to any of the claims 1 through 8,
in that the carrier substrate (TS) is a low-warpage LTCC ceramic.

10. Component according to any of the claims 1 through 9,
in that, on the underside of the carrier substrate (TS), SMD-capable connection metallizations (KO) are provided that are connected via feedthroughs (DK) with wirings (LB) arranged between two layers (US, OS) of the at least two-layer carrier substrate, with wirings (LB) between individual connection areas (AF), or are directly connected with the connection areas.

11. Component according to any of the claims 1 through 10,
in that the chip (CH) is metallized at least in the region of its lower edge, and the carrier substrate (TS) is metallized at least on a band below the lower edge of the chip, whereby the metallization comprises at least one of the metals Al, Ni, Cu, Pt or Au.

12. Component according to any of the claims 1 through 11,
in that a lacquer layer that is selectively removed to generate an inscription is applied over the entire back side of the chip (CH).

13. Component according to claim 12,
in that an additional layer forming an optical contrast with the lacquer layer is provided under the lacquer layer.

14. Component according to any of the chips 1 through 13,
in that the outer edges of the chip (CH) canted, such that the chip tapers towards the carrier substrate (TS).

15. Method for production of an encapsulated component,
- in that a multi-layer carrier substrate (TS) is provided which comprises recesses (AN) of the depth (h1) in which solderable connection areas (AF) are uncovered,
- in that a chip (CH) comprising component structures (BS) on one surface as well as solderable metallizations (LM) connected with these is provided,

- in that, on the surface of the chip or of the carrier substrate, a depression (VT) of the depth (h2) is generated for acceptance of the component structures of the height (h3),
- in that, on the solderable connection areas or the solderable metallizations, bumps (BU) of a height (h4) are generated, whereby

$$h4 > (h1 + h2)$$

- in that the chip (CH) is attached and soldered to the carrier substrate (TS) in flip-chip arrangement, such that the solderable connection areas (AF) are connected via the bumps (BU) with the solderable metallizations (LM), and
- whereby, upon mutual sinking of the bumps conditional upon the melting, the chip drops to the height (h1 + h2) on the carrier substrate and rests there
- whereby component structures (BS) are arranged in a hollow of the height (h2) formed by the depression (VT) and covered by chip or carrier substrate.

16. Method according to claim 15,

- in that a first contact metallization (M) is generated on the carrier substrate (TS) in the region below the lower chip edge,
- in that a second contact metallization is generated on the chip (CH) in the region between the contact area and the facing chip areas,
- in that a solder border (LR) circling the chip is generated for connection of first and second contact metallization.

17. Method according to claim 15 or 16,

in that a chip narrowing towards the surface with the component structures with canted side edges is used,

in that the solder border is generated on the carrier substrate before the attachment of the chip,

in that upon soldering the side edges of the chip are attached with metallizations located there to the solder border and are soldered therewith.

18. Method according to claim [sic] 15 through 17,
in that the bumps (BU) are generated on the solderable metallizations (LM) of the chip (CH) or on the solderable connection areas (AF) of the carrier substrate (TS) via

a) galvanic deposition
b) silk screen or stencil printing
c) scraping of solder paste into the recesses of the carrier substrate
d) vibration of solder balls into the recesses
e) laser bumping
f) stamping of solder foil over the recesses.

19. Method according to claim [sic] 15 through 18,
in that a carrier substrate (TS) comprises at least an upper and a lower layer (US) is used, and in that, for the solderable connection areas (AF) in the lower layer, recesses are generated, filled with conductive material and, as necessary, provided with a solderable coating that constitutes the solderable connection areas (AF) that are uncovered in the recesses (AN) of the upper layer (OS).

20. Method according to claim [sic] 15 through 19,
in that the base of the recesses (AN) is selected larger in the upper layer than the area of the solderable connection areas (AF) on the surface of the lower layer (US), in that the cross-section of the bumps (BU) is selected smaller than those of the recesses (AN).

21. Method according to any of the claims 15 through 20,
in that, after the soldering and the generation of the solder border (LR), material is removed from the back side of the chip (CH) with the aid of a particle beam method or via abrasion, and the chip is thus thinned.

22. Method according to any of the claims 15 through 21,

in that the chips (CH) are applied in use [sic] to a large-area carrier substrate (TS), and are first subsequently isolated into components or modules via division of the carrier substrate between the chips.

23. Method according to claim 22,
in that the isolation ensues via a beam method in which the solder border (LR) serves as a mask.

24. Method according to any of the claims 15 through 23, in that a multi-layer ceramic is used as a carrier substrate (TS),
in that the recesses (AN) are generated in the upper layer (OS) of the multi-layer ceramic before the sintering and are filled with a filling material,
in that the filling material is removed again after the sintering.

25. Method according to claim 24,
in that one of the following method combinations is selected for the filling of the recesses (AN) and the removal of the filling materials again:

a) filling with Al_2O_3 and removal of the Al_2O_3 with a beam process
b) filling with PbO and removal of the PbO via dissolution with acetic acid
c) filling with carbon-containing materials and removal of the carbon-containing materials via dissolution with acetic acid.

26. Method according to any of the claims 15 through 25,
in that the bonding of the bumps (BU) to the solderable metallizations (LM) is improved by one of the following steps a or b

c) [sic] roughening of the chip surface before the application of the metallizations in the region of the solderable metallizations,
d) [sic] structured application of the metallizations such that an open band-like, grid-like or sieve-like structure of the solderable metallizations is created, in whose openings the chip is uncovered.